Listing of Claims

1. (Currently Amended) A method for forming a CMOS well structure, comprising:

forming a first mask on a substrate, the first mask having a plurality of openings ;

forming a plurality of first conductivity type wells over the substrate, each of the plurality of first conductivity type wells being formed by filling ~~in a~~ respective openings in the first mask with first conductivity type material;

forming a cap over each of the first conductivity type wells;

removing the first mask;

forming sidewall spacers on sidewalls of each of the first conductivity type wells; and

forming a plurality of second conductivity type wells over the substrate, each of the plurality of second conductivity type wells being formed by filling spaces between respective first conductivity type wells with second conductivity type material.

2. (Original) The method of claim 1, further comprising:

forming a plurality of shallow trench isolations between the first conductivity type wells and second conductive type wells;

forming at least one second conductivity type MOS device inside each of the plurality of first conductivity type wells; and

forming at least one first conductivity type MOS device inside each of the plurality of second conductivity type wells.

3. (Original) The method of claim 1, wherein the plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process.

4. (Original) The method of claim 1, wherein the first mask is a low-temperature chemical vapor deposition nitride.

5. (Original) The method of claim 1, wherein the thickness of the first mask is in the range of about 50 nm to about 500 nm.

6. (Original) The method of claim 3, wherein the step of forming a plurality of first conductivity type wells comprises forming a first epitaxial layer in-situ doped with a first conductivity dopant.

7. (Original) The method of claim 6, wherein the doping concentration of the first conductivity dopant is in the range of about 1 X $10^{17}/cm^3$ to about 1 X $10^{20}/cm^3$.

8. (Original) The method of claim 6, further comprising:

forming the first epitaxial layer to a larger thickness than that of the first mask to avoid epitaxial faceting; and

etching back the first epitaxial layer to a smaller thickness than that of the first mask.

9. (Original) The method of claim 3, wherein the step of forming a plurality of second conductivity type wells comprises forming a second epitaxial layer in-situ doped with a second conductivity dopant.

10. (Original) The method of claim 9, wherein the doping concentration of the second conductivity dopant is in the range of about 1 X $10^{17}/cm^3$ to about 1 X $10^{20}/cm^3$.

11. (Original) The method of claim 9, further comprising:

forming the second epitaxial layer to a larger thickness than that of the first conductivity type wells to avoid corner faceting; and

planarizing the second epitaxial layer.

12. (Original) The method of claim 1, wherein step of forming a cap comprises thermal oxidation.

13. (Original) The method of claim 1, wherein the step of forming sidewall spacers comprises chemical vapor deposition.

14. (Original) The method of claim 1, wherein the sidwall spacers are made of nitride.

15. (Original) The method of claim 1, wherein the thickness of the sidewalls spacers is in the range of about 5 nm to about 30 nm.

16. (Original) The method of claim 1, wherein the first conductivity type is n-type and the second conductivity type is p-type.

17. (Original) The method of claim 1, further comprising:

etching the substrate between the plurality of openings in the first mask to a predetermined depth before forming a plurality of first conductivity type wells over the substrate.

18. (Original) The method of claim 17, further comprising:

forming a plurality of first conductivity type implant regions in the substrate before the step of forming sidewall spacers, each of the plurality of first conductivity type implant regions formed in a respective exposed surface of the substrate.

19. (Original) The method of claim 18, wherein the plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process over exposed surfaces of the first conductivity type implant regions.

20. (Original) The method of claim 17, wherein the predetermined depth is in the range of about 20 nm to about 500 nm.

21. (Original) The method of claim 18, wherein a doping concentration of the first conductivity type implant regions are in the range of about 1 X $10^{19}/cm^3$ to about 1 X $10^{21}/cm^3$.

22. (Original) The method of claim 18, wherein the plurality of first conductivity type implant regions are formed in the substrate to a depth of about 20 nm to about 600 nm.

23. (Original) The method of claim 19, wherein at least one of the plurality of first conductivity type wells is a dummy first conductivity well that terminates at least one second conductivity type well.

24. (Original) The method of claim 19, wherein at least one of the plurality of second conductivity type wells is a dummy second conductivity well that terminates at least one first conductivity type well.

25. (Original) The method of claim 19, wherein the first conductivty type is n-type and the second conductivity type is p-type.

26. (Currently Amended) A CMOS well structure, formed by a method comprising:

forming a first mask on a substrate, the first mask having a plurality of openings ;

forming a plurality of first conductivity type wells over the substrate, each of the plurality of first conductivity type wells being formed by filling ~~in a~~ respective openings in the first mask with first conductivity type material;

forming a cap over each of the first conductivity type wells;

removing the first mask;

forming sidewall spacers on sidewalls of each of the first conductivity type wells; and

forming a plurality of second conductivity type wells over the substrate, each of the plurality of second conductivity type wells being formed by filling spaces between respective first conductivity type wells with second conductivity type material.

27. (Original) The CMOS well structure of claim 26, wherein the method further comprises:

forming a plurality of shallow trench isolations between the first conductivity type wells and second conductive type wells;

forming at least one second conductivity type MOS device inside each of the plurality of first conductivity type wells; and

forming at least one first conductivity type MOS device inside each of the plurality of second conductivity type wells.

28. (Original) The CMOS well structure of claim 26, wherein the plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process.

29. (Original) The CMOS well structure of claim 26, wherein the substrate between the plurality of openings in the first mask is etched to a predetermined depth before forming a plurality of first conductivity type wells over the substrate.

30. (Original) The CMOS well structure of claim 29, wherein a plurality of first implant regions are formed in the substrate before the step of forming sidewall spacers, each of the plurality of first conductivity type implant regions formed in a respective exposed surface of the substrate.

31. (Original) The CMOS well structure of claim 30, wherein the plurality of first conductivity type wells are formed by a first selective epitaxial growth process, and the plurality of second conductivity type wells are formed by a second selective epitaxial growth process over exposed surfaces of the first conductivity type implant regions.

32. (Original) The CMOS well strucutre of claim 26, wherein the first conductivty type is n-type and the second conductivity type is p-type.

33. (Canceled)

34. (Canceled)